# San José State University
# Department of Electrical Engineering
# EE-222, Advanced Integrated Devices, Section 01, Fall, 2020

## Course and Contact Information

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|---|---|
| Instructor: | Dr. Hiu Yung Wong |
| Office Location: | Online (Zoom) |
| Telephone: | 408-924-3910 |
| Email: | hiuyung.wong@sjsu.edu |
| Office Hours: | Mon: 9:00am-10:30am, Wed: 3:00pm-4:30pm, or by appointment |
| Class Days/Time: | Monday and Wednesday 4:30pm-5:45pm |
| Classroom: | Online (Zoom) |
| Prerequisites: | Graduate standing or instructor approval |

## Course Description

Complementary Metal-Oxide Semiconductor (CMOS) device scaling; Silicon-On-Insulator (SOI) and 3D transistor technologies; Device modeling and simulation; Surveys on Wide-Band-Gap power electronics; 3D and cross-point memories, neuromorphic computing, opto-electronics and superconductor electronics.

## Course Format

### Technology Intensive and Hybrid Class

This class has 2 lectures per week. The students are expected to have stable internet access to attend the online lectures through Zoom. The students need to have Webcam installed on their computer and be able to use LockDown Browser by Respondus to take quizzes and exam. Their computers should be compatible to remote desktop to access the servers in the campus. **Please see the following for more details.**

## Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Learning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU on Spartan App Portal http://one.sjsu.edu to learn of any updates. For help with using Canvas see Canvas Student Resources page (http://www.sjsu.edu/ecampus/teaching-tools/canvas/student_resources)

## Course Learning Outcomes:

CLO1: Describe and explain the scaling history and challenges (geometric scaling, High-k / metal gate-, strain-, SiGe channel-, 3D device-augmented scaling, and hyperscaling)

CLO2: Simulate novel devices using TCAD tool

CLO3: Describe the operating principles and limitations of UTB-SOI, FinFET and Nanowire

CLO4: Describe the basic operating principles of emerging memories and trade-offs

CLO5: Describe the operating principles of emerging devices (such as Tunnel FET, Negative Capacitance FET)

## Required Texts/Readings

### Textbook

Lecture notes and selected review paper

### Other Recommended Readings

- CMOS and Beyond: Logic Switches for Terascale Integrated Circuits, Tsu-Jae King Liu and Kelin Kuhn,Editors, Cambridge University Press, 2015
- Elements of Quantum Computing, Seiki Akama, Springer, 2015
- FinFETs and Other Multi-Gate Transistors, J.-P. Colinge, Spring, 2015
- Device and Circuit Cryogenic Operation for Low Temperature Electronics, Francis Balestra and G. Ghibaudo, Editors, Springer, 2001
- Introduction to Superconducting Circuits, A. M. Kadin, John Wiley & Sons, 1998
- Inside NAND Flash Memories, R. Micheloni, L. Crippa, A. Marelli, Springer, 2010
- Semiconductor Devices: Physics and Technology, 2nd Edition by S. M. Sze, John Wiley, 2001

### Software

TCAD Sentaurus (Available in EE Synopsys Lab Linux machines)

## Course Requirements and Assignments

Students are expected to attend all classes and participate actively in the seminar, submit the assignments and project reports on time and attend the mid-term and final exams. Assignments and Project Reports must be submitted on time to receive full credit. Late submission of Assignments and Project Reports within 3 days after the due date will only receive half of the credits. No credits will be given after the late submission due date (i.e. 3 days after the due date).

Review the following policy about your responsibility:

- Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

"Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus."

### Project

The project has 3 phases. Depending on the project difficulty, it can be either individual or team project. In the first phase, students will read literature paper and choose the topics. In the second phase, students will perform

TCAD simulations to design transistors. In the third phase, after discussing with the lecturer, students will improve their design.

**Final Examination or Evaluation**

Exams will be closed book. However, students are allowed to bring a calculator and a page of aid sheet. There will be no make-up exam, except for reasons allowed by the University Policy, and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. The course is based on letter grading and grading percentage breakdown is as follow:

## Grading Information

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|---|---|
| Assignment | 10% |
| Midterm Exam | 15% |
| Final Exam | 25% |
| Design Project | 50% |

**Determination of Grades**

- Every assignment has equal weight

**Grading Breakdown:**
A = 100 to 93 points
A minus = 92 to 88 points
B plus = 87 to 84 points
B = 83 to 79 points
B minus = 78 to 75 points
C plus = 74 to 72 points
C = 71 to 69 points
C minus = 68 to 65 points
D plus = 64 to 62 points
D = 61 to 59 points
D minus = 58 to 55 points
F = 55 points or lower

## Classroom Protocol

Students are required to be in class on time. Students are welcome to ask questions through chat box or interrupting the lecturer. However, students should only discuss issues related to the class.

## University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

## EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:
• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam

• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor."

**Measures Dealing with Occurrences of Cheating**

• Students who are suspected of cheating during an exam will be referred to the Student Conduct and Ethical Development office and depending on the severity of the conduct, will receive a zero on the assignment or a grade of F in the course. Grade Forgiveness does not apply to courses for which the original grade was the result of a finding of academic dishonesty.
• Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
• A student's second offense in any course will result in a Department recommendation of suspension from the University.

**Proctoring Software and Exams**

Exams will be proctored in this course through Respondus Monitor and LockDown Browser. Please note it is the instructor's discretion to determine the method of proctoring. If cheating is suspected the proctored videos may be used for further inspection and may become part of the student's disciplinary record. Note that the proctoring software does not determine whether academic misconduct occurred, but does determine whether something irregular occurred that may require further investigation. Students are encouraged to contact the instructor if unexpected interruptions (from a parent or roommate, for example) occur during an exam.

**Recording Zoom Classes**

This course or portions of this course (i.e., lectures, discussions, student presentations) will be recorded for instructional or educational purposes. The recordings will only be shared with students enrolled in the class through Canvas. If, however, you would prefer to remain anonymous during these recordings, then please speak with the instructor about possible accommodations (e.g., temporarily turning off identifying information from the Zoom session, including student name and picture, prior to recording).

**Students are not allowed to record without instructor permission**

Students are prohibited from recording class activities (including class lectures, office hours, advising sessions, etc.), distributing class recordings, or posting class recordings. Materials created by the instructor for the course (syllabi, lectures and lecture notes, presentations, etc.) are copyrighted by the instructor. This university policy (S12-7) is in place to protect the privacy of students in the course, as well as to maintain academic integrity through reducing the instances of cheating. Students who record, distribute, or post these materials will be referred to the Student Conduct and Ethical Development office. Unauthorized recording may violate university and state law. It is the responsibility of students that require special accommodations or assistive technology due to a disability to notify the instructor.

**Technology Requirements**

Students are required to have an electronic device (laptop, desktop or tablet) with a camera and built-in microphone and speaker/headphone. SJSU has a free equipment loan program available for students.

Students are responsible for ensuring that they have access to reliable Wi-Fi during tests. If students are unable to have reliable Wi-Fi, they must inform the instructor, as soon as possible

or at the latest one week before the test date to determine an alternative. See Learn Anywhere website for current Wi-Fi options on campus.

**Zoom Classroom Etiquette**

1. Mute Your Microphone: To help keep background noise to a minimum, make sure you mute your microphone when you are not speaking.

2. Be Mindful of Background Noise and Distractions: Find a quiet place to "attend" class, to the greatest extent possible.
3. Avoid video setups where people may be walking behind you, people talking/making noise, etc.
4. Avoid activities that could create additional noise, such as shuffling papers, listening to music in the background, etc.
5. Limit Your Distractions/Avoid Multitasking: You can make it easier to focus on the meeting by turning off notifications, closing or minimizing running apps, and putting your smartphone away (unless you are using it to access Zoom).
6. Use Appropriate Virtual Backgrounds: If using a virtual background, it should be appropriate and professional and should NOT suggest or include content that is objectively offensive or demeaning.

**Online Exams**
**Testing Environment: Setup**

1. No earbuds, headphones, or headsets visible.
2. The environment is free of other people besides the student taking the test.
3. If students need scratch paper for the test, they should present the front and back of a blank scratch paper to the camera before the test.
4. No other browser or windows besides Canvas opened.
5. A workplace that is clear of clutter (i.e., reference materials, notes, textbooks, cellphone, tablets, smart watches, monitors, keyboards, gaming consoles, etc.)
6. Well-lit environment. Can see the students' eyes and their whole face. Avoid having backlight from a window or other light source opposite the camera.
7. Personal calculator is allowed.

**Testing Environment: Scan**
Before students can access the test questions, they are expected to conduct a scan around their testing environment to verify that there are no materials that would give the student an unfair advantage during the test. The scan will include:

1. the desk/work-space
2. a complete view of the computer including USB ports and power cord connections
3. a 360-degree view of the complete room

**Students must:**
1. Remain in the testing environment throughout the duration of the test.
2. Keep full face, hands, workspace including desk, keyboard, monitor, and scratch paper, in full view of the webcam

**Technical difficulties**

**Internet connection issues:**
Canvas autosaves responses a few times per minute as long as there is an internet connection. If your internet connection is lost, Canvas will warn you but allow you to continue working on your exam. A brief loss of internet connection is unlikely to cause you to lose your work.
However, a longer loss of connectivity or weak/unstable connection may jeopardize your exam.

**Other technical difficulties**:
Immediately email the instructor a current copy of the state of your exam and explain the problem you are facing. Your instructor may not be able to respond immediately or provide technical support. However, the copy of your exam and email will provide a record of the situation.

Contact the SJSU technical support for Canvas:

Technical Support for Canvas Email: ecampus@sjsu.edu Phone: (408) 9242337

If possible, complete your exam in the remaining allotted time, offline if necessary. Email your exam to your instructor within the allotted time or soon after.

# EE-222 / Advanced Integrated Devices, Fall 2020, Course Schedule***

****The schedule is subject to change with advanced notice on Canvas.*

| Week | Seminar | Assignment | Project |
|---|---|---|---|
| 17-Aug | No Class | | |
| 19-Aug | Overview of Scaling | | |
| 24-Aug | Review of MOSFET Device Physics | | |
| 26-Aug | Short Channel Effect | | |
| 31-Aug | Short Channel Effect | | |
| 2-Sep | SOI | Assignment 1 due on 9/6 | |
| | Labor Day - No Class | | |
| 7-Sep<br>9-Sep | SOI | | Project phase 1 Due |
| 14-Sep | FinFET and multi-gate devices | | |
| 16-Sep | FinFET and multi-gate devices | | |
| 21-Sep | Nanowire/Nanosheet/DTCO | | |
| 23-Sep | Modern CMOS Technology | Assignment 2 due on 9/27 | |
| 28-Sep | Modern CMOS Technology | | |
| 30-Sep | Wide-Bandgap Power Devices | | |
| | Wide-Bandgap Power Devices | | |
| 5-Oct<br>7-Oct | NCFET | Assignment 3 due on 10/11 | |
| 12-Oct | Review | | |
| 14-Oct | Midterm | | |
| 19-Oct | Tunnel FET | | |
| 21-Oct | Tunnel FET | | |
| 26-Oct | 3D Flash Memory | | Project phase 2 Due |
| 28-Oct | ReRAM/PCM | | |
| 2-Nov | ReRAM/PCM | | |
| 4-Nov | STT RAM | | |
| | STT RAM | | |
| 9-Nov<br>11-Nov | Veteran's Day – No Class | Assignment 4 due on 11/15 | |

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| 16-Nov | Neuromorphic computing | | |
| 18-Nov | Superconducting Electronics | | |
| 23-Nov | Superconducting Electronics | | |
| 25-Nov | Non-Instructional Day | | |
| 30-Nov | Quantum Computing | | |
| 2-Dec | Project Presentation | | Project Phase 3 Due |
| 7-Dec | Project Presentation / Review | | |
| Final Exam | Final Exam Wednesday, December 9 1445-1700 | | |