Electrical Engineering Research Seminar

Title: _Efficient FPGA implementations of Machine Learning Algorithms_

Speaker: Prof. Philip Leong, University of Sydney

Time: 11:00am to noon, May 10 (Friday), 2019

Location: ENG 292

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Abstract: Efficient FPGA implementations of Machine Learning Algorithms

FPGA implementations of machine learning algorithms have been shown to be extremely efficient when the problem fits entirely on the FPGA but it remains a challenge to scale to problems of interest to industry. In this talk, our recent research on how to increase the capacity of existing approaches will be described.

In the first part of the talk we will describe an implementation of the Fastfood algorithm for scaling up online kernel methods. By utilizing the theory of random projections, problems with 1000x larger input dimension and dictionary size can be solved. A systolic implementation that operates at 500 MHz clock frequency was achieved. The next part of the talk describes how the resource requirements in convolutional neural networks can be reduced using symmetric quantisation (SYQ), which achieves state of the art accuracy for binary and ternary weights. Finally, a new DSP-block architecture, optimised for energy-efficient embedded machine learning will be presented.

Speaker Bio: Philip Leong received the B.Sc., B.E. and Ph.D. degrees from the University of Sydney. In 1993 he was a consultant to ST Microelectronics in Milan, Italy working on advanced flash memory-based integrated circuit design. From 1997-2009 he was with the Chinese University of Hong Kong. He is currently Professor of Computer Systems and Deputy Head of School in the School of Electrical and Information Engineering at the University of Sydney. His other roles include Senior Visitor Scholar at Fudan University, Visiting Professor at Imperial College, Visiting Professor at Harbin Institute of Technology, and Chief Technology Advisor to ClusterTech. He is currently on sabbatical at Xilinx Research Labs.