SJSU SAN JOSÉ STATE UNIVERSITY

Charles W Davidson College of Engineering · Electrical Engineering

Cryogenic Nanoelectronics Section 01

EE 226

Spring 2024 3 Unit(s) 01/24/2024 to 05/13/2024 Modified 01/12/2024

Contact Information

Instructor:	Dr. Hiu Yung Wong
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Office Hours:	MW 6:30-7:30pm (online or in person) or by appointment

Course Description and Requisites

Introduces the cryogenic nanoelectronics used in emerging technologies, such as quantum computers. The cryogenic and room temperature properties of the devices and circuits will be discussed and contrasted. Design skills of nanoelectronics devices and circuits at cryogenic temperature will be emphasized.

Prerequisite(s): Graduate standing or instructor consent.

Letter Graded

Classroom Protocols

Students are required to be in class on time and no use of cell phone during the class.

Course Learning Outcomes (CLOs)

Upon successful completion of this course, students will be able to:

CLO1: identify the technical challenges and opportunities in cryogenic electronics

CLO2: explain, model and summarize the new device physical phenomena appear at cryogenic temperature

CLO3: explain and summarize how to manipulate quantum computer qubit with CMOS compatible circuits

CLO4: compare the difference between room temperature and cryogenic temperature devices and circuits

CLO5: Able to perform cryogenic device simulation using commercial TCAD

CLO6: Able to design, simulate and analyze cryogenic circuits using commercial tools

Course Materials

Textbook

- No textbook required.

Other Readings

- Practical Cryogenics: An Introduction to Laboratory Cryogenics, Nicholas Howard Balshaw, Oxford Instruments (UK), 1996.
- Quantum Transport: Introduction to Nanoscience, Y. V. Nazarov, and Y. M. Blanter, Cambridge University Press, 2009. (available in both a print and multi-user e-book version through the SJSU library collection)
- Device and Circuit Cryogenic Operation for Low Temperature Electronics, Editors: Balestra, Francis, Ghibaudo, G. (Eds.), Springer US, 2001
- Design of Analog CMOS Integrated Circuits, 2nd Edition, Behzad Razavi McGraw-Hill, 2017
- RF Microelectronics, 2nd Edition, Behzad Razavi Prentice Hall, 2012

Library Liaison: Jane Dodge: jane.dodge@sjsu.edu

Course Requirements and Assignments

Prerequisites:	Graduate standing or with instructor consent

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Learning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU on Spartan App Portal http://one.sjsu.edu to learn of any updates. For help with using Canvas see Canvas Student Resources page.

Course Requirements and Assignments

Students are expected to attend all classes and participate actively in the seminar, submit the assignments and project reports on time and attend the mid-term and final exams. Assignments and Project Reports must be submitted on time to receive full credit. Late submission of Assignments and Project Reports within 3 days after the due date will only receive half of the credits. No credits will be given after the late submission due date.

Review the following policy about your responsibility:

- Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

"Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus."

Course Project

Students can choose either using TCAD to optimize FinFET/SOI/Planar CMOS/BJT at 4.2K or using 14nm FinFET or 45nm technology to design LNA for 77K or lower temperature applications.

✔ Grading Information

Final Examination or Evaluation

Exams will be closed book. However, students are allowed to bring a calculator and a page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. The course is based on letter grading and the grading percentage breakdown is as follow:

Grading Information

Assignment	30%
Midterm Exam	20%
Final Exam	20%

Project 30%

Determination of Grades

- Every assignment has equal weight (totally 30% of the final score)
- Assignment and Project reports must be submitted on time to receive full credit. Late submission: Half of the credit will be given if submitted within 3 days after the due date. No credit will be given if submitted after the late submission due date.

Grading Breakdown:

A = 100 to 93 points

A minus = 92 to 88 points

B plus = 87 to 84 points

B = 83 to 79 points

B minus = 78 to 75 points

C plus = 74 to 72 points

C = 71 to 69 points

C minus = 68 to 65 points

D plus = 64 to 62 points

D = 61 to 59 points

D minus = 58 to 55 points

F = 55 points or lower

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given

- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

• A student's second offense in any course will result in a Department recommendation of suspension from the University.

University Policies

Per University Policy S16-9 (PDF) (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on the Syllabus Information (https://www.sjsu.edu/curriculum/courses/syllabus-info.php) web page. Make sure to visit this page to review and be aware of these university policies and resources.

Course Schedule

Class Days/Time:	Monday and Wednesday 7:30 pm-8:45 pm
Classroom:	Dudley Moorhead Hall 234

****The schedule is subject to change with advance notice on Canvas.*

Week		Seminar	Assignment	Project
1	22-Jan	No Class		
	24-Jan	Introduction/ Cryogenic Basics		

2	29-Jan	Cryogenic Bulk MOSFET		
	31-Jan	Cryogenic Bulk MOSFET		
3	5-Feb	Cryogenic Bulk MOSFET		
	7-Feb	Cryogenic SOI		
4	12-Feb	Cryogenic SOI		
	14-Feb	FinFET	Assignment 1 due on 2/18	
5	19-Feb	Cryogenic FinFET		
	21-Feb	Cryogenic FinFET/ Layout		
6	26-Feb	HEMT		
	28-Feb	Cryogenic HEMT		
7	4-Mar	Quantum Effects		
	6-Mar	Quantum Effects	Assignment 2 due on 3/10	
8	11-Mar	Quantum Effects and Review		
	13-Mar	Midterm		
9	18-Mar	Noise Analysis		
	20-Mar	Noise Analysis		Project Start

10	25-Mar	Noise Analysis		
	27-Mar	Noise Analysis		
11	1-Apr	Spring Recess		
	3-Apr	Spring Recess		
12	8-Apr	Cryogenic Low Noise Amplifier		
	10-Apr	Cryogenic Low Noise Amplifier	Assignment 3 due on 4/17	
13	15-Apr	Cryogenic Low Noise Amplifier		
	17-Apr	Cryogenic Low Noise Amplifier		
14	22-Apr	Qubit Control/Sensing Device/Circuits		
	24-Apr	Qubit Control/Sensing Device/Circuits		
15	29-Apr	Qubit Control/Sensing Device/Circuits		
	1-May	Qubit Control/Sensing Device/Circuits		Project due
16	6-May	Project Presentation		
	8-May	Project Presentation	Assignment 4 due on 5/10	
17	13-May	Review		
Final Exam	15-May	Wednesday, May 15, 7:45-10:00 PM		