SJSU SAN JOSÉ STATE UNIVERSITY

College of Science · Computer Science

Computer Architecture

CS 147

Fall 2026 In Person 3 Unit(s) 08/19/2026 to 12/07/2026 Modified 08/19/2026

Contact Information

Instructor: Dr. Faramarz Mortezaie

Email: faramarz.mortezaie@sjsu.edu

Office Hours

Tuesday, 12:30 PM to 1:30 PM, online: zoom

Zoom Link: https://sjsu.zoom.us/j/86252633056

Course Description and Requisites

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Prerequisite(s): CS 47 or CMPE 102 (with a grade of "C-" or better), Computer Science, Applied and Computational Math, Forensic Science: Digital Evidence, or Software Engineering majors only; or instructor consent.

Letter Graded

Classroom Protocols

Attendance

Students are expected to attend the lectures and participate in the discussion.

Instructors may drop students from class if they fail to attend respond to instructor email.

Technical Difficulties and Internet Connection issues

Canvas AutoSaves responses a few times per minute if there is an internet connection. If your internet connection is lost, Canvas will warn you but allow you to continue working on your exam. A brief loss of internet connection is unlikely to cause you to lose your work. However, a longer loss of connectivity or weak/unstable connection may jeopardize your exam. Other technical difficulties: Immediately email the instructor a current copy of the state of your exam and explain the problem you are facing. Your instructor may not be able to respond immediately or provide technical support. However, the copy of your exam and email will provide a record of the situation.

Contact the SJSU technical support for Canvas:

Technical Support for Canvas

Email: ecampus@sjsu.edu

Phone: (408) 924--2337

https://www.sjsu.edu/ecampus/support/

If possible, complete your exam in the remaining allotted time, offline if necessary. Email your exam to your instructor within the allotted time or soon after.

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Program Information

Diversity Statement - At SJSU, it is important to create a safe learning environment where we can explore, learn, and grow together. We strive to build a diverse, equitable, inclusive culture that values, encourages, and supports students from all backgrounds and experiences.

Course Learning Outcomes (CLOs)

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instructions set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing cost-effective methods of increasing hardware performance are.
- Appreciate how computer-aided design tools and hardware description languages can be used to verify and measure the performance of hardware design

Course Materials

Textbook Information

Publisher: zyBooks

1. Sign in or create an account at learn.zybooks.com

2. Enter zyBook code: SJSUCS147MortezaieFall2026

3. Subscribe

A subscription is **$97**. Students may begin subscribing on Aug 05, 2026 and the cutoff to subscribe is Nov 27, 2026. Subscriptions will last until Dec 25, 2026.

Course Requirements and Assignments

SJSU classes are designed such that to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

University policy F69-24 at http://www.sjsu.edu/senate/docs/F69-24.pdf states, "Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading."

Descriptions of Assignments/Exams

No late work is accepted.

Exams: Exams will be in the form of multiple choice, short answer, and programming/coding questions and will be based on the individual assignments and course material. The exams are individual work with closed books/handouts/laptops/calculators.

A course schedule is provided towards the end of this document providing a tentative schedule for Labs, Project and Exams. This schedule is subject to change with fair notice.

✓ Grading Information

Criteria

Homework, Weekly Quiz, discussion	25%
Exam-1	25%
Exam-2	25%
Comprehensive Final Exam	25%

Breakdown

A+	98 – 100%
A	93 – 97%
A-	90 – 92%

B+ B B-	88 – 89% 83 – 87% 80 – 82%
C+ C C-	78 – 79% 73 – 77% 70 – 72%
D+ D D-	68 – 69% 63 – 67% 60 – 62%
F	59% and less

University Policies

Per University Policy S16-9 (PDF) (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on the Syllabus Information (https://www.sjsu.edu/curriculum/courses/syllabus-info.php) web page. Make sure to visit this page to review and be aware of these university policies and resources.

Course Schedule

TTH 7:30 AM - 8:45 AM

Duncan Hall 450

When	Topic	Notes
Lecture Week-1 08/20/2026 7:30 AM - 8:45 AM	Introduction and number systems	Understand binary and hexadecimal number systems, and be able to perform conversions and simple arithmetic operations. 2's complements

When	Topic	Notes
Lecture Week-2 08/24/2026 7:30 AM - 8:45 AM	Instructions: Language of the Computer	Chapter 2
Lecture Week-3 08/31/2026 7:30 AM - 8:45 AM	Instructions: Language of the Computer	Chapter 2
Lecture Week-4 09/07/2026 7:30 AM - 8:45 AM	Instructions: Language of the Computer CISC vs. RISC	Chapter 2
Lecture Week-5 09/14/2026 7:30 AM - 8:45 AM	Adders and Carry Look ahead adders Multipliers and Dividers	Chapter 3
Lecture Week-6 09/21/2026 7:30 AM - 8:45 AM	Review and Exam-1	Note: Exam-1 Date: Sept-24 at 9:00 am
Lecture Week-7 09/28/2026 7:30 AM - 8:45 AM	Arithmetic For Computers Floating Points and Floating Points instructions	Chapter 3
Lecture Week-8 10/05/2026 7:30 AM - 8:45 AM	Combinational and sequential Circuits with VHDL	Chapter 3 and Appendix A

When	Topic	Notes
Lecture Week-9 10/12/2026 7:30 AM - 8:45 AM	Building a Datapath	Chapter 4
Lecture Week-10 10/19/2026 7:30 AM - 8:45 AM	Building a Datapath	Chapter 4
Lecture Week-11 10/26/2026 7:30 AM - 8:45 AM	Pipelining and parallelism The processor and Processor Design	Chapter 4
Lecture Week-12 11/02/2026 7:30 AM - 8:45 AM	Review and Exam-2	Note: Exam-2 Date: Nov-5 at 9:00 am
Lecture Week-13 11/09/2026 7:30 AM - 8:45 AM	Memory Hierarchy: Cache	Chapter 5
Lecture Week-14 11/16/2026 7:30 AM - 8:45 AM	Memory Hierarchy: Virtual Memory Management	Chapter 5
Lecture Week-15 11/23/2026 7:30 AM - 8:45 AM	Memory Hierarchy: Virtual Memory Management	Chapter 5 Note: Thursday Nov-26 No Class (No Instruction Day)

When	Topic	Notes
Lecture Week-16 11/30/2026 7:30 AM - 8:45 AM	Project Presentations and Review	Final Exam Review
Final Exam 12/15/2026 8:30 AM - 10:30 AM	Closed Book Final Exam	Note: Final Exam Date is Tuesday Dec-15 8:30 AM - 10:30 AM