SJSU SAN JOSÉ STATE UNIVERSITY

College of Science · Computer Science

Computer Architecture Section 01

CS 147

Spring 2025 In Person 3 Unit(s) 01/23/2025 to 05/12/2025 Modified 01/28/2025

Contact Information

Instructor(s):	Dr. Chung-Wen (Albert) Tsao
Office Location:	MH411
Email:	chung-wen.tsao@sjsu.edu (Once the class starts, use Canvas Inbox)
Class Days/Time:	T/R 10:30AM - 11:45AM (Section 01) T/R 1:30PM - 2:45PM (Section 03)
Classroom:	Duncan Hall 318 (Section 01) Science Building 311 (Section 03)
Office Hours:	T/R/F 3:30pm-4:30pm at MH411 or on ZOOM at https://sjsu.zoom.us/j/82400634761

Course Description and Requisites

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Prerequisite(s): CS 47 or CMPE 102 (with a grade of "C-" or better), Computer Science, Applied and Computational Math, Forensic Science: Digital Evidence, or Software Engineering majors only; or instructor consent.

Letter Graded

Classroom Protocols

- Instructor may drop students (by the Instructor Drop Deadline) who
  - are absent for 1st day of class without informing you before 2nd day of class, or
  - have no proof of the prerequisite fulfillments.
- Do NOT share/post online any course materials, PPT slides, or homework solutions.
- Use of electronic devices during exams is NOT allowed unless stated otherwise.
- You are required to check Canvas for reading/assignments.
- The information on this syllabus is subject to change; changes, if any, will be clearly explained in class, and it is your responsibility to become aware of them.
- Once the class starts, use Canvas Inbox to email me for a faster response. I check the Canvas Inbox emails much more often than my school emails.

Class Format

- Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas at http://sjsu.instructure.com.
- You are responsible for regularly checking the most updated messages and uploaded materials there.

Program Information

Diversity Statement - At SJSU, it is important to create a safe learning environment where we can explore, learn, and grow together. We strive to build a diverse, equitable, inclusive culture that values, encourages, and supports students from all backgrounds and experiences.

Course Goals

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLOs)

Upon successful completion of this course, students will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.
- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.

- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

Course Materials

Computer Organization and Design – The Hardware/Software Interface, 5th

- **Author:** David A. Patterson, John L. Hennessy
- **Publisher:** Elsevier
- **Edition:** 5th
- **ISBN:** 9780124077263

Required Textbooks

Logic & Computer Design Fundamentals

- **Author:** Mano & Kime
- **Publisher:** PEARSON
- **Edition:** 5th
- **ISBN:** 9780131989269

Optional**Textbooks**

Course Requirements and Assignments

Assignments:

- No late submission of assignments will be accepted except for the verified emergency such as doctor's notes or family death certificates.
- All homework must clearly indicate each student’s name, course, and assignment number.
- Students are allowed (and actively encouraged) to form study groups.
- You may discuss solutions, but you MUST write up the answers independently.
- If you use a website or reference book, you must cite it.

- If there are multiple similar submissions not exhibiting independent thought, or with words obviously lifted from a book or website, ALL such submissions will receive scores of 0.

LockDown Browser + Webcam Requirement:

This course requires the use of LockDown Browser and a webcam for online quizzes. The webcam can be the type that's built into your computer or one that plugs in with a USB cable. Watch this brief video to get a basic understanding of LockDown browser and the webcam feature. Download and install LockDown browser from here.

Pop Quizzes:

- Pop quizzes locked with passcode may be given anytime during class.
- They are usually explained in class and most of them will be due on the end of the class.
- The purpose of pop quizzes is to encourage you to and reinforce the concepts we learned in lectures.

Midterm and Final Examinations:

There will be two midterm examinations, and a cumulative final exam.

- All the students need to attend synchronously.
- No make-up exams for anyone except for the verified emergency with the official documents.
- Use of electronic devices during exams is NOT allowed unless stated otherwise.
- All exams may include quizzes (closed book) or written test (open book) or both.
- All exams will remain with the instructor.

✔ Grading Information

1. Final grades will not be adjusted in any way - so an 89.99% is still a B+.
2. No incomplete grades will be given.
3. Do not ask for special treatment. The rules for this course apply to everyone equally.
4. Cheating will not be tolerable; a ZERO will be given to any cheated assignment/exams, and it will be reported to the Department and the University.

Note that "All students have the right, within a reasonable time, to know their academic scores, to review their grade- dependent work, and to be provided with explanations for the determination of their course grades."

See University Policy F13-1 at http://www.sjsu.edu/senate/docs/F13-1.pdf for more details.

Breakdown

- Pop quizzes 10%
- Homework 15%

- Project 30%
- Midterm 1 15%
- Midterm 2 15%
- Final Exam 15%

Criteria

The grading scale is as follows:

100% - 97.00%	A+
96.99% - 94.00%	A
93.99% - 90.00%	A-
89.99% - 87.00%	B+
86.99% - 84.00%	B
83.99% - 80.00%	B-
79.99% - 77.00%	C+
76.99% - 74.00%	C
73.99% - 70.00%	C-
69.99% - 67.00%	D+
66.99% - 64.00%	D
63.99% - 60.00%	D-
below 60.00%	F

University Policies

Per University Policy S16-9 (PDF) (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant university policy concerning all courses, such as student responsibilities, academic integrity, accommodations, dropping and adding, consent for recording of class, etc. and available student services (e.g. learning assistance, counseling, and other resources) are listed on the Syllabus Information (https://www.sjsu.edu/curriculum/courses/syllabus-info.php) web page. Make sure to visit this page to review and be aware of these university policies and resources.

Course Schedule

Course Schedule (This schedule is subject to change. Any change will be communicated via Canvas with fair notice.)

Week	Date	Topics	
1	1/24	Syllabus, Introduction	
2	1/29, 1/31	Logic Design	
3	2/4, 2/6	Logic Design	
4	2/11, 2/13	Combinational Circuit Design	
5	2/18, 2/20	Combinational Circuit Design	
6	2/25, 2/27	Sequential Circuit Design	
7	3/4, 3/6	Sequential Circuit Design	
8	3/11, 3/13	MIPS Instructions	
9	3/18, 3/20	Review, Midterm 1	

10	3/25, 3/27	MIPS Instructions	
	4/1, 4/3	Spring Recess	
11	4/8, 4/10	The Processor	
12	4/15, 4/17	The Processor	
13	4/22, 4/24	Memory Hierarchy	
14	4/29, 5/1	Review, Midterm 2	
15	5/6, 5/8	Memory	
Final Exam	Section 01	Monday, May 19 10:45 AM-12:45 PM (https://www.sjsu.edu/classes/final-exam-schedule/spring-2025.php)	
Final Exam	Section 03	Tuesday, May 20 1:00-3:00 PM (https://www.sjsu.edu/classes/final-exam-schedule/spring-2025.php)	

Other important dates.

Thu, Feb 20	◦ Late Add Post Census Request Requirement begins ◦ Late Drop/ Semester Withdrawal Petition Requirement begins: Undergraduate (https://sjsu.edu/ue/student-petitions/drops/index.php), Graduate (https://www.sjsu.edu/cgs/current-students/forms/withdrawal-form-instructions.php)
Fri, March 21	Graduation Application Deadline to Qualify for Priority Registration (https://www.sjsu.edu/registrar/graduation/application-central.php) for Undergrads

Mon-Fri, March 31 - April 4	Spring Recess - no classes
Mon, March 31	Cesar Chavez Day - Campus Closed
Thu, April 22	◦ Last Day to File Late Drop/ Semester Withdrawal Petition: Undergraduate (https://sjsu.edu/ue/student-petitions/drops/index.php), Graduate (https://www.sjsu.edu/cgs/current-students/forms/withdrawal-form-instructions.php) ◦ Last day to submit Late Enrollment Post Census for current semester
Mon, May 12	◦ Last Day of Instruction ◦ Last Day to Complete Coursework for "Incomplete Grades"
Tue, May 13	Faculty Web Access for Grade Posting Opens at 8 am
May 14-16 May 19-21	Culminating Activities & Final Examination Period (https://www.sjsu.edu/classes/final-exam-schedule/spring-2025.php)