San José State University
Department of Computer Science
CS147, Computer Architecture, Section 2, Fall, 2019

Course and Contact Information

Instructor: Fabio Di Troia

Office Location: DH282

Telephone:

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Office Hours: Thursday, 17:30 – 19:30

Class Days/Time: TuTh 9:00AM - 10:15AM

Classroom: MH 233

Prerequisites: CS 47 or CMPE 102 or equivalent (with a grade of "C-" or better)

Course Format

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Leaning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU at http://my.sjsu.edu (or other communication system as indicated by the instructor) to learn of any updates.

Course Description

Introduction to the basic concepts of computer hardware structure and design, including processors and arithmetic logic units, pipelining, and memory hierarchy.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

- Understand the role of each major hardware component of a computer system and their synergistic interaction with each other and software.
- Analyze and perform tradeoffs between the cost, performance, and reliability of alternative computer architectures.

- Understand, analyze, and design digital logic structures for the basic combinational and sequential circuits.
- Understand the alternative binary internal representation of information (such as sign-magnitude, one's complement, two's complement, and floating point) along with their optimizations and tradeoffs.
- Be able to perform basic mathematical operations (add, multiply) in the various Boolean number representation schemes.
- Understand the operation of, and be able to analyze from a cost/performance standpoint, certain optimized hardware structures.
- Appreciate the need to use a memory hierarchy and understand how locality of memory referencing in typical programs can be leveraged to perform effective memory architecture management.
- Understand and emulate the various mapping, replacement, and dynamic memory allocation algorithms for cache and virtual memory management.
- Understand the rationale and philosophy behind both complex instruction set computers (CISC) and reduced instruction set computers (RISC), and the tradeoffs between the two architectures.
- Understand how pipelining and parallel processing are cost-effective methods of increasing hardware performance.

Required Texts/Readings

Textbook

COMPUTER ORGANIZATION and DESIGN – The Hardware/Software Interface | Edition: 5th
Authors: David A. Patterson, John L. Hennessy
ISBN: 9780124077263
Publication Date: 10/10/2013
Publisher: ELSEVIER

Other Readings

COMPUTER ARCHITECTURE | Edition: 5th
Author: John L. Hennessy
ISBN: 9780123838728
Publication Date: 09/29/2011
Publisher: ELSEVIER

COMPUTER ORGANIZATION and ARCHITECTURE | Edition: 10th
Author: Stallings
ISBN: 9780134101613
Publication Date: 01/12/2015
Publisher: PEARSON

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

Homework, Midterm and Final exam are expected for this class. Homework is due on Canvas by class starting time on the due date. Each assigned problem requires a solution and an explanation (or work) detailing how you arrived at your solution. Cite any outside sources used to solve a problem. When grading an assignment, I may ask for additional information.

NOTE that University policy F69-24 at http://www.sjsu.edu/senate/docs/F69-24.pdf states that "Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading."

Final Examination or Evaluation

The final examination consists in designing a complete CPU datapath capable to fetch, decode and execute specific instructions.

Grading Information

- Homework, 25%
- Midterm 1, 25%
- Midterm 2, 25%
- Final Project, 25%

Note that "All students have the right, within a reasonable time, to know their academic scores, to review their grade-dependent work, and to be provided with explanations for the determination of their course grades." See University Policy F13-1 at http://www.sjsu.edu/senate/docs/F13-1.pdf for more details.

Determination of Grades

Semester grade will be computed as a weighted average of the 3 scores listed above.
No make-up tests or quizzes will be given and no late homework (or other work) will be accepted. Also, in-class work must be completed in the section that you are enrolled in.

Nominal Grading Scale:

Percentage	Grade
92 and above	A
90 – 91	A-
88 – 89	B+
82 – 87	B
80 – 81	B-
78 – 79	C+
72 – 77	C
70 – 71	C-
68 – 69	D+
62 – 67	D
60 - 61	D-
59 and below	F

Classroom Protocol

- **Cheating** will not be tolerated.
- Student must be respectful of the instructor and other students. For example, No disruptive or annoying talking.
- Turn off cell phones
- Class begins on time
- Valid picture ID required at all times

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

CS147 / Computer Architecture, Fall 2019, Course Schedule

This schedule is subject to change. Any change will be communicated via Canvas with fair notice.

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	08/22	Introduction
1	08/27	Introduction
2	08/29	MIPS Instructions
2	09/3	MIPS Instructions
3	09/5	MIPS Instructions
3	09/10	MIPS Instructions
4	09/12	Arithmetic for Computers
4	09/17	Arithmetic for Computers
5	09/19	Arithmetic for Computers
5	09/24	Wrap-up
6	**09/26**	**Midterm 1**
6	10/01	Logic Design
7	10/03	Logic Design
7	10/08	The Processor
8	10/10	The Processor
8	10/15	The Processor
9	10/17	The Processor
9	10/22	The Processor
10	10/24	The Processor
10	10/29	Wrap-up
11	**10/31**	**Midterm 2**
11	11/05	Memory Hierarchy
12	11/07	Memory Hierarchy
12	11/12	Memory Hierarchy
13	11/14	Memory Hierarchy
13	11/19	Memory Hierarchy
14	11/21	Memory Hierarchy
14	11/26	TBD

Week	Date	Topics, Readings, Assignments, Deadlines
15	12/3	TBD
15	12/5	Wrap-up
Final Exam	12/16	Time: 7:15 – 9:30am